MachZ Errata

Summary of Errata for the 1.5 MachZ chip

Bug	Fix	Description
09	SW Document	The primary and secondary HDD traps do not work.
10	SW Document	GPT1 cannot be re-triggered by HDD activity.
22	Document	During PCI bus target memory read, with a fast decode target, the South Bridge doesn't generate the correct address and/or correct transaction type if the target retries the transaction, w/o data transferred.
27	SW Document	PCI Lock Does Not Work. A PCI Master can not lock the SDRAM to prevent CPU access. The CPU can not perform a lock to PCI Bus.
28	SW Document	Multiple SMI's on one source.
29	Document	Buffer alignment causes IDE DMA to hang.
32	2.1	Nine pins fail the Human Model for ESD.
35	Document	S.B. repeats DWORD on long bursted reads if PCIC-DISC_ON_LN_BOUNDARY = 0

P/N 9140-0004-00

MachZ Programming/Hardware Considerations

The following issues need to be considered when writing code or designing with the MachZ chip:

Tracking Number: MACHZ_009

Date Opened: 02/24/2000
System Configuration: Clock speed = 33MHz
Multiplier = 2
PCI Video Card
64MB/4 = 16MB
BIOS Rev: Dated: 02/15/2000 alfa1
Software (if applicable): CSDIAG in conjunction with test smihandler
Environment: Room

Bug Description: The primary and secondary HDD traps do not work. When F0 Index 82[0] is set, a read to 1F7h should generate a SMI. This does not happen. When F0 Index 83[6] is set, a read to 177h should generate a SMI. This does not happen. These are used in conjunction with the HDD timers to allow power management of the device. Normal operation is to set up a timer and if the timer expires then the power management code, via SMI, is entered and the device is powered down. At the time of power down the trap is enabled, so that if there is an access to the device, the power management code is entered again and device operation can be resumed.

Tracking Number: MACHZ_010

Date Opened: 02/24/2000
System Configuration: Clock speed = 33MHz
Multiplier = 2
PCI Video Card
64MB/4 = 16MB
BIOS Rev: Dated: 02/15/2000 alfa1
Software (if applicable): CSDIAG in conjunction with test smi handler
Environment: Room
Bug Description: GPT1 cannot be re-triggered by HDD activity.

General Purpose Timer 1 (GPT1), F0 Index 88h and its associated control register, F0 Index 89h can be used as a way to enter a SMI handler based on a set time. There are also many ways to re-trigger the timer based on system activity, i.e. an access to COM1. The GPT1 in MachZ cannot be re-triggered by HDD activity, which ties into Bug 009. All other re-trigger sources work.

Tracking Number: MACHZ_022

Date Opened: 03/03/00
System Configuration: MachZ Mode 0 Validation Board
BIOS Rev: ALPHA 4
Software (if applicable):
Environment: Room

Bug Description: During PCI bus target memory read, with a fast decode target, the South Bridge doesn't generate the correct address and/or correct transaction type when the if the target retries the transaction, w/o data transferred. This behavior can only be introduced using a test card. There are no known commercial boards with the capability of responding within one clock pulse.

Tracking Number: MACHZ_027

Date Opened: 7 March 2000
System Configuration: MachZ Verification Board
BIOS Rev:
Software (if applicable):
Environment: Room

Bug Description: PCI Lock Does Not Work

A PCI Master can not lock the SDRAM to prevent CPU access. The CPU can not perform a lock to PCI Bus. However, the CPU can perform an explicate lock operation to SDRAM which prevents PCI Master access.

Tracking Number: MACHZ_028

Date Opened: 03/17/2000
System Configuration: Clock speed = 33MHz
Multiplier = 2
PCI Video Card
64MB/2 = 32MB
BIOS Rev: Dated: 03/15/2000 alfa7
Software (if applicable): CSDIAG
Environment: Room

Bug Description: Multiple SMI's on one source.

When the SMI is cleared in the handler by performing a read on the top level Read-To-Clear status regs, the SMI goes inactive then active again. The 486 processor latches this transition when the handler resumes from the original SMI it immediately reenters but there is no pending source. This behavior does not threaten system operation as long as the handler can handle spurious SMI's. It s a performance issue.

Tracking Number: MACHZ_029

Date Opened: 03/17/2000
System Configuration: Clock speed = 33MHz
Multiplier = 2
PCI Video Card
64MB/2 = 32MB
BIOS Rev: Dated: 03/15/2000 alfa7
Software (if applicable): CSDIAG (ide tests)
Environment: Room

Bug Description: Buffer alignment causes IDE DMA to hang.

This failure is when the DMA is set up to read data from SDRAM and write the data to hard disk. If the read buffer is not on a 32 byte boundary the IDE bus master engine will move the first 16 bytes and then lock up. The only recovery is a reset. This failure does not occur if the data is read from the hard drive and mastered into the SDRAM.

Tracking Number: MACHZ_035

Date Opened: 05/08/00

BIOS Rev: Beta\EVAL1

Bug Description: The SB repeats DWORDS during long bus master memory reads, if the Bus Master inserts an average of 3 IRDY waits (Core=33MHz, CPU=3x, PCI=1x) or 2 IRDY waits (Core=66MHz, CPU =2x, PCI = 0.5x). This bug has only been observed with the HP E2925B PCI Bus Exerciser, and not with a real Bus Mastering Card.

NOTE: Setting Bit 3- DISC_ON_LN_BOUNDARY, in the PCIC register can eliminate this bug. This was confirmed during the HP E2925B bus exerciser testing. This breaks up the transaction, such that SB FIFO problem doesn't occur. It is recommended to leave this bit clear, unless there is a real bus master card that exhibits this behavior.

Failing Conditions:

1) Perform a 256 DWORD bursted read from SDRAM, with the HP E2925B bus Exerciser. Program the HP E292B to insert (3 or 2) IRDY waits for each data phase.

2) A repeated DWORD occurred between 107 to 256 DWORD's transferred following a single address phase. These numbers are not absolute, but convey the relative occurrence of the problem.

Register Settings:
1) Burst enabled. PCIC(11Bh) CPU2PCI_BURST_EN = 1, PCIM2DRM_BRST_EN = 1 and BM_BURSTRD_ALWYS = 1.
2) Prefetch disabled. SNOOPCTRL(11Dh) DIS_EM_PREFETCH = 1.
3) CPU/PCI concurrency enabled. SNOOPCTRL(11Dh) DIS_CONCURRENCY = 0.
4) Write Back Merge disabled. SNOOPCTRL(11Dh) WB_MERGE = 1.

MachZ Version 1.5 Errata

The following issues need to be considered when using MachZ silicon at level 1.5. The following defects are corrected with 2.1 silicon scheduled for availability in 1Q2000:

Tracking Number: MACHZ_032

Date Opened: 03/24/00
System Configuration: None
BIOS Rev: NA
Bug Description: Nine pins on the MachZ chip do not meet the human interface model for ESD. Proper ESD precautions must be taken when mounting the devices on the board.

The following pins failed 1KV and should be rated at 500v:

NAMEPIN	
VBAT	AD03
khz32_c	AE01
khz_32c_c	AF01
por_disB19	
port1_m	AF13
port1_pAE13	
port2_m	AE14
port2_pAF14	
usb_pwr	AF15